library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

entity convertor is

port( a3,a2,a1,a0:in bit;

b3,b2,b1,b0:out bit);

end convertor;

architecture arh2421 of convertor is

begin

b3 <= a2 and a1;

b2 <= (a2 and not(a1))+(a3 and not(a2));

b1 <= a3 xor a1;

b0 <= a0;

end arh2421;